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Comprehensive Assessment of Avalanche Operating Boundary of SiC Planar/Trench MOSFET in Cryogenic Applications

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***Abstract*— The avalanche ruggedness of power devices becomes a crucial issue to ensure the safe operation of the power conversion systems, particularly under the extreme temperature conditions. In this paper, the avalanche capability of SiC planar/trench MOSFETs is systematically evaluated and analyzed over the temperature range of 90 to 340 K. Importantly, the essential mechanisms and temperature dependence of avalanche failure under cryogenic conditions are further explored by combining many analysis methods such as TCAD simulations, the unclamped inductive switching characterizations, and the transient junction temperature prediction. The highest avalanche energy density of 171.24 mJ/mm^2 at 90K indicates the great application potential of SiC planner MOSFET in cryogenic electronics. Moreover, the safe avalanche operation boundary (AOB) model is established over the cryogenic temperature range. The relevant analysis method and AOB model can be used to accurately evaluate and quantitatively predict the avalanche capability of SiC planar/trench MOSFETs for the cryogenic converter design.**

Keywords—1.2 kV SiC planar MOSFET, 1.2 kV SiC trench MOSFET, Unclamped inductive switching (UIS), Avalanche capability, Cryogenic temperature.

I. INTRODUCTION

In power conversion systems, the ruggedness of switching devices is extremely important and critical to sustain unexpected situations, such as short circuit, voltage overshoot, surge current, etc. [1]-[3] The avalanche shock is one of the most serious issues of reliability, which is caused by the parasitic inductance of power circuits referred to as the avalanche failure [4]-[5].

For the traditional high-voltage power switch, due to the presence of a negative differential resistance (NDR) behavior of Si IGBT, the filamentary current conduction locally increases the current density causing early device latch-up and possible device failure, resulting in that the IGBT is less robust to avalanche operation[6].

The SiC power devices are regarded as an ideal candidate to increase power density and efficiency in high power conversion systems [7]-[9]. However, higher *dv/dt* and *di/dt* of SiC power devices will introduce more serious avalanche failure issues. To date, the failure mechanism and operation robustness of avalanche performance have not been fully studied for SiC power devices, especially under extreme temperature conditions [10]-[11].

In order to explore the avalanche capability of SiC MOSFETs, some research has been carried out at a high-temperature scale [12]-[21]. For high-temperature SiC MOSFET modules and discrete devices, the avalanche current has been proved to be equal to the rated current at 25 °C [12]-[14]. While the maximum energy dissipation of SiC MOSFET shows a negative temperature coefficient, supported with the measurements under 25 °C, 75 °C, 90 °C and 150 °C conditions [15]. The avalanche capability and failure mechanisms of SiC MOSFETs are also evaluated based on the internal junction temperature, where the critical transient junction temperature peak can be elevated up to 687 °C for 1.2 kV SiC DMOSFETs [16]-[18]. As peak junction temperature yields result well above the failure limit of aluminum contacts, an avalanche failure of 1.2 kV SiC MOSFETs occurs [19]. Furthermore, to illustrate the temperature dependence of BJT latch-up mechanism, an electrothermal model is developed based on the finite-element simulations over a temperature range of -25 to 125 °C [12],[20]. Particularly, the BJT latch-up of SiC MOSFETs is triggered by the body diode reverse recovery process, with high *dv/dt* over a temperature range of -75 to 175°C [21].

Comparing to high-temperature applications, the cryogenic applications shows higher requirements for the avalanche reliability of power switches due to wide temperature range, high system integration, and difficult-to-replace components [22]-[23]. Although the static and dynamic characteristics of SiC MOSFET are analyzed under cryogenic condition [24]-[25], the avalanche performance of SiC MOSFETs has been rarely analyzed at cryogenic temperature. A comprehensive evaluation and analysis of the SiC MOSFETs' avalanche

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capability will help improve the reliability of the SiC-based energy conversion system under cryogenic temperature.

In this paper, based on a customized self-built single pulse unclamped inductive switching characterization platform, the avalanche performance of 1.2 kV SiC planar and trench MOSFETs is systematically evaluated and analyzed over the temperature range of 90 to 340 K for the first time. The main contributions of this paper are listed as follows:

1) The essential cause of avalanche failure mechanisms for SiC planar/trench MOSFETs is further explored at cryogenic temperature. Combining with various analysis methods, including the TCAD simulations, the avalanche failure mechanisms of two SiC MOSFETs are validated as the latch-up of parasitic BJT and the gate oxide degeneration. Importantly, the design approaches from the chip and circuits level are proposed to improve the avalanche capability of two SiC MOSFETs.

2) The temperature dependence of the above two avalanche failure mechanisms are comprehensively evaluated and quantified over the temperature range of 90 to 340 K. The larger temperature coefficient of avalanche capability indicates that SiC MOSFET has great potential for cryogenic applications.

3) An avalanche capability model of SiC MOSFET is proposed to define the safe avalanche operation boundary (AOB) under the cryogenic conditions. The analysis method and avalanche performance model can be used to accurately evaluate and quantitatively predict the avalanche capability of SiC planar/trench MOSFETs, which has important application value for the design of cryogenic converters.

II. Unclamped Inductive Switching Measurements

The single pulse unclamped inductive switching (UIS) circuit, as illustrated in Fig. 1, is widely used to characterize the avalanche performance of power switches [26]-[27]. In this work, the device under test (DUT) is connected in series with a inductor (L = 5.886 mH), while a 42.3 μF capacitor (namely C_{dc}) is paralleled with a programmable dc power supply (V_{dc}) to maintain constant bus voltage during the UIS transient. The transient avalanche current flowing through the DUT is measured by a coaxial current shunt (CVR) (SSDN-414-01) with 400 MHz band-pass. Signal pulse generated by a pulse function arbitrary generator is sent to a driver board to control the state of the DUT.

To extract the avalanche performance over the cryogenic temperature range, a liquid nitrogen thermostat system is designed, as shown in Fig. 2. The TPS-Compact Turbopump provides a vacuum environment for a copper plate, which locates inside the Cryogenic Vacuum Chamber and is cooled by liquid nitrogen. The vacuum environment could avoid the influence of water vapor in the air. The temperature controller can achieve precise temperature control of the copper plate. The temperature control accuracy is 0.1 K over the temperature range of 77 to 340 K. In this temperature control unit, only the DUT is connected with While the rest of the circuit components and characterization equipment operate at room temperature. The above hardware design can ensure the characterization system normally operates and accurately measures the temperature dependence of DUTs by eliminating the influence of temperature on other components.

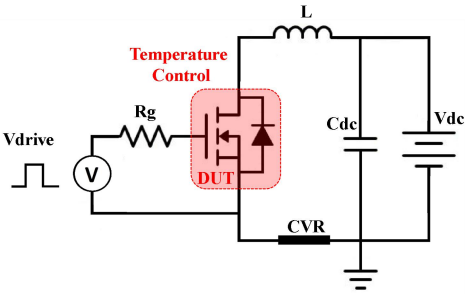

Fig. 1 Equivalent circuit schematic of single pulse unclamped inductive switching (UIS) measurement.

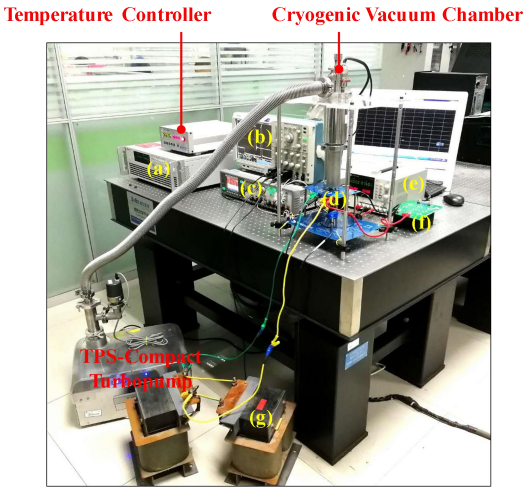

Fig. 2 Cryogenic temperature characterization hardware set-up with (a) programmable DC power supply, (b) digital phosphor oscilloscope, (c) pulse function arbitrary generator, (d) PCB board, (e) auxiliary power supply, (f) DC link capacitor, (g) power inductor.

As shown in Fig. 3, the UIS could been divided into four phase, not only for the normal avalanche switching but the avalanche failure. The off-state DUT sustains the DC bus voltage during the phase A. Once the DUT is turned on by a high gate driver voltage during the phase B, the on-state DUT results in a charging process of the power inductor (L) until to the desired avalanche current value. The desired avalanche current value can be obtained by adjusting the pulse duration. During the phase C, the voltage across the power inductor rapidly increases when the DUT is turned off again. The high voltage forces the DUT into avalanche operation mode. In this phase, the avalanche current flowing though the DUT linearly decreases and releases the energy stored in the inductor. According to the strength of the avalanche current, the SiC MOSFET will enter two different avalanche modes. Under a small avalanche current condition (21.5 A), as shown in Fig. 3(a), the avalanche current decreases to zero, showing as a normal avalanche mode. In contrast, the transient avalanche current decreases first and then increases again when the peak of avalanche current are large as 22.0 A, as shown in Fig. 3(b). The above avalanche process indicates the avalanche failure mode, resulting in an unrecoverable device damage.

To quantitatively evaluate the avalanche capability of SiC MOSFETs, two critical parameters, peak avalanche current (I_{avp}) and avalanche energy (E_{av}), are used. The I_{avp} can be obtained directly from the measurement data. The E_{av} is

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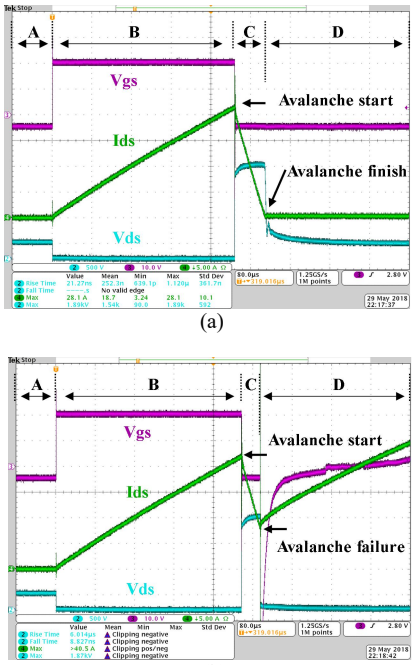

Fig. 3 Measured (a) normal avalanche waveforms and (b) avalanche failure waveforms of commercial SiC MOSFET (manufactured by Cree, C2M0080120D) at room temperature. Purple, green and blue solid lines denote gate-source voltage, drain current, and drain-source voltage, respectively. Scale: V_{gs} => 10 V/div, I_{ds} => 5 A/div, V_{ds} => 500 V/div. Measured: avalanche current is 21.5 and 22.0A. Calculated: avalanche energy ae 1.36 and 1.42J.

derived by calculating the time integral of the product of avalanche voltage and avalanche current, as follows:

$$E_{av} = \int I_{ds} \bullet V_{ds} dt \qquad (1)$$

where the integration interval is the duration of avalanche state, as illustrated with phase C in Fig. 3.

Using above UIS characterization platform, the temperature dependence of the avalanche capability of SiC planar/trench MOSFETs can be accurately measured over the temperature range of 90 to 340 K. Furthermore, the relevant measurement results help to establish a safe avalanche operating boundary (AOB) under the cryogenic temperature.

III. Physical Analysis of Avalanche Failure

The avalanche capability of SiC MOSFET is affected by various factors, such as semiconductor material, cell structure, manufacture process, package form, etc. Each factor would contribute to different avalanche failure mechanisms. In this section, the impact of structure differences on avalanche capability of SiC plana/trench MOSFET is comparatively analyzed based on the finite element simulation. Although the lack of 3D boundary conditions does not allow for quantitative interpretation of results, the 2D TCAD simulations can qualitatively illustrate the internal electrical characteristics of SiC MOSFETs.

A. Avalanche analysis of SiC Planar MOSFET

1) Physical detail inside the planar MOSFET

To explore the physical details inside SiC planar MOSFET, a typical half-cell structure model is established with

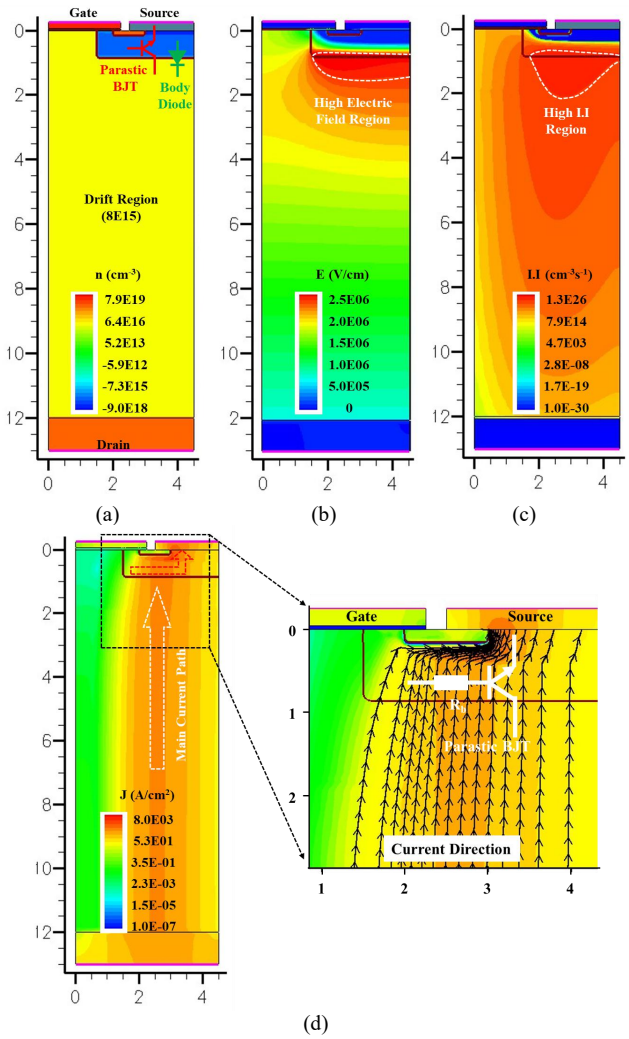

Fig. 4 The typical half-cell structure model and simulation results for SiC planar MOSFET with the mixed circuits simulation method, including (a) the critical structure parameters, (b) the electric filed distribution, (c) the impact ionization (I.I) distribution, and (d) the avalanche current distribution

Sentaurus TCAD software, as shown in Fig. 4(a). Clearly, the N+ source region, P-body region, and N drift region together form a parasitic NPN bipolar junction transistor (BJT). Meanwhile, the P-body region and N drift region constitute a parasitic body diode.

Theoretical assumptions and literature data (see [28]-[29]) are used to define doping and dimensions. This paper focuses on the avalanche performance of SiC MOSFET, so the reverse avalanche breakdown voltage of the model is the most critical parameter. By adjusting doping concentration and thickness of drift region, the model could sustain nearly 1.8 kV breakdown voltage, corresponding to the actual experimental results. The doping concentration of drift region is 8e15 cm^{-3}. The doping concentration of channel region and P-body region are 1.5e17 and 3.5e17 cm^{-3}, respectively. The doping concentration of the N+ source region, the P+ source region and the substrate are 1e19 cm^{-3}. The critical geometric parameters of SiC planar MOSFET are shown in TABLE I.

Although the model parameters may not be identical to that of the commercial MOSFET used in the UIS characterization,

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TABLE I
THE DIMENSION PARAMETERS OF SIC PLANAR MOSFET

Parameter	Value (μm)
Channel length	0.45
JFET region width	1.5
P+ region width	1.5
Half-cell width	4.5
SiO_2 layer thickness	0.05
Height of N+ region	0.15
Height of P_{body} region	0.60
Epitaxial layer thickness	12
Substrate thickness	1

it can reflect the basic structure of the real device. The simulation results qualitatively describe the internal electrical characteristics of the SiC MOSFET in avalanche mode.

Avalanche performance of SiC planar MOSFET is extracted with mixed circuits simulation method. The circuit parameters used in the mixed circuits model are same as that of the actual UIS characterization. The average value of peak avalanche current density is set to 1.27 A/mm^2. While the MOSFET operates as avalanche conduction mode, the $P_{body}N_{drift}$ junction corresponds to the highest electric field region (> 2.5 MV/cm), as shown in Fig. 4(b). The impact ionization rate (I.I) is usually used to quantify the avalanche ionization strength. The I.I distribution inside the SiC planar MOSFET is shown in Fig. 4(c). In the high I.I region (I.I > 1.1e26 /(cm^{3}s)), a large number of electron-hole pairs are orientated by the high electric field and eventually produce the avalanche current.

As shown in Fig. 4(d), the majority avalanche current flows vertically through the $P_{body}N_{drift}$ junction, then horizontally through the interior of the P-body region, and finally to the source contact. Due to the body resistance (R_b) and the horizontal current component inside the P-body region, a voltage drop (V_{base}) occurs across the P-body region. Once the V_{base} is higher than the built-in potential (V_{bi}) of $P_{body}N_{drift}$ junction, the parasitic BJT would be triggered on, resulting in an avalanche failure, eventually.

2) Temperature performance during UIS

The overlap of high electric field region and high current density region causes a great of heat generation, resulting in a dramatic temperature increase inside the MOSFET. As illustrated in Fig. 5, the area on the right side of the $P_{body}N_{drift}$ junction will be continuously heated during the UIS duration, which causes a hot point inside the power MOSFET.

Since the R_b and V_{bi} have positive and negative temperature coefficients respectively, the latch-up condition of parasitic BJT continues to change during the whole avalanche duration. Clearly, a higher transient junction temperature corresponds to a lower critical avalanche current density.

3) Limitation analysis of avalanche capability

Based on the above TCAD simulation and analysis, two avalanche failure mechanisms potentially contribute to the avalanche failure of SiC planar MOSFET: the latch-up of the parasitic BJT and the unrecoverable thermal damage associated with the hot point. For the BJT latch-up, the trigger

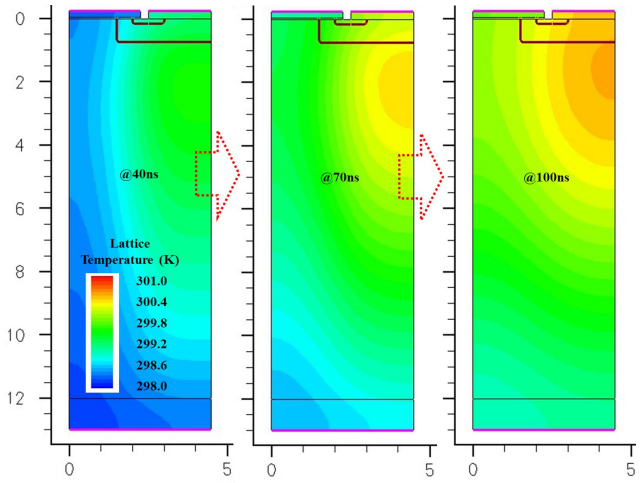

Fig. 5 The lattice temperature distribution of SiC planar MOSFET at 40, 70, and 100 ns after the MOSFET operates with avalanche state during the UIS process.

condition is that V_{base} is higher than V_{bi} of $P_{body}N_{source}$ junction, which is closely dependent on the junction temperature and avalanche current density. The higher temperature and larger avalanche current density will be more likely trigger a failure case. For the unrecoverable thermal damage, this implies that the transient temperature inside the device exceeds the critical transition temperature of the semiconductor material or the melting point of packaging materials. For SiC material, the transition temperature is 1308.15 K (1035 °C), corresponding to n_i of 1.4e14 /cm^3. The melting point of aluminum is 660.3 °C.

The above two avalanche failure mechanisms are closely related to the maximum temperature inside the MOSFET. As whichever mechanism ultimately causes an avalanche failure, it fully depends on the critical temperature condition of which failure mechanism is met first during the UIS process.

The simulation results indicate that the avalanche capability of the SiC planar MOSFET can be enhanced from two aspects. One is to optimize the power cell parameters for a uniformed temperature distribution on the chip level, the other is to reduce the operation temperature for a larger temperature margin to reach the temperature limit.

B. Avalanche Performance analysis of SiC Trench MOSFET

1) Physical detail inside the trench MOSFET

The typical half-cell structure of SiC trench MOSFET is established with Sentaurus TCAD software, as shown in Fig. 6(a). Although the device structure is different from the planar MOSFET, there is still a parasitic NPN BJT, consisting of n+ source region, P-body region, and N drift region.

The breakdown voltage of the simulation model is designed at approximately 1665 V using a 12 μm-thick n-type epitaxial layer with the doping concentration of 8e15 cm^{-3}. The doping concentration of the P-body region and P-well region are 1.5e17 and 3.5e17 cm^{-3} [28]-[29], respectively. The doping concentration of N+ source region, P+ source region, and substrate are 1e19 cm^{-3}. The critical geometric parameters of SiC trench MOSFET are shown in TABLE II.

Based on the above TCAD model, the avalanche performance of SiC trench MOSFET is extracted with the

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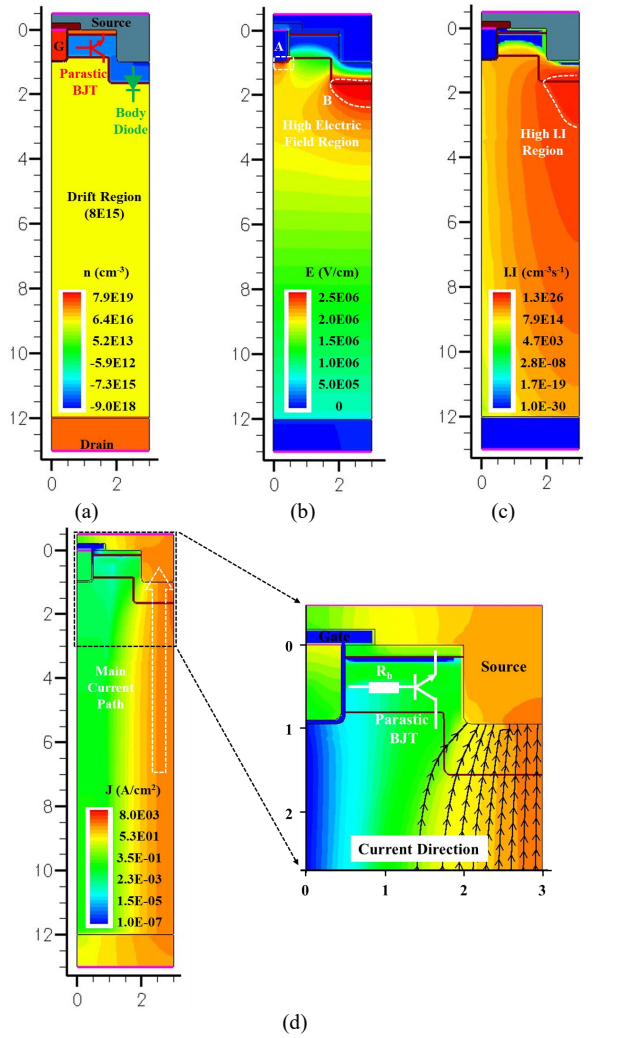

Fig. 6 The typical half-cell structure model and simulation results of SiC trench MOSFET with the mixed circuits simulation method, including (a) critical structure parameters, (b) electric filed distribution, (c) impact ionization (I.I) distribution, and (d) avalanche current distribution

mixed circuit simulation method. Although the double trench structure reduces the electric field at the gate oxide to a certain extent, that does not completely eliminate the occurrence of high electric field. Different from the electric field distribution of SiC planar MOSFET, the maximum electric strength region appears at the bottom of the gate oxide and the bottom of source trench region, as shown in Fig. 6(b). Correspondingly, the high impact ionization rate region (I.I >1.3e26 /(cm^{3}s)) occurs at the bottom of source trench region, as shown in Fig. 6(c). The corner of the gate oxide is the second-highest region of the I.I inside the MOSFET.

As illustrated in Fig. 6(d), most of avalanche current flows vertically through the $P_{body}N_{drift}$ junction at the bottom of the trench source, while little avalanche current flows horizontally through the interior of the P-body region, and finally to the source contact. As the small V_{base} cannot trigger the parasitic BJT, the avalanche current distribution indicates that the avalanche failure mechanism related to BJT latch-up is not suitable for the SiC trench MOSFET.

2) Temperature performance during UIS

TABLE II
THE DIMENSION PARAMETERS OF SIC TRENC MOSFET

Parameter	Value (μm)
Polysilicon gate width	0.50
N+ region width	1.5
P-well width	1.25
Half-cell width	4.5
SiO_2 layer thickness	0.05
Polysilicon gate height	1.0
N+ region thickness	0.15
P_{body} region height	0.75
P-well height	1.0
Epitaxial layer thickness	12
Substrate thickness	1

Similar to the planar MOSFET, the overlap of the high electric field and current density region causes a hot point at the upper part of the drift region near the trench source. The temperature inside the trench MOSFET dramatically increases during the UIS duration.

The positive temperature coefficient of avalanche voltage implies that the electric field is gradually enhanced during the UIS process. Correspondingly, the gate oxide corner suffers a higher electric field and temperature stress during the whole UIS process.

3) Limitation analysis of avalanche capability

Based on the above TCAD simulation and analysis, there are three potential mechanisms contributing to the avalanche failure of SiC trench MOSFET, the latch-up of parasitic BJT, the unrecoverable thermal damage, and the degradation of the gate oxide. As the lack of the avalanche current component flowing horizontally inside the P-body region, the parasitic BJT is hard to be triggered on. In comparison, the dramatic temperature increase inside the MOSFET will be more likely to introduce unrecoverable thermal damage or gate oxide degradation.

For UIS characterization, the gate oxide corners are simultaneously exposed to the high electric fields and high temperatures, which degrades the reliability of the gate oxide. As the most vulnerable position inside the trench MOSFET, the gate oxide corner may be firstly destroyed under the avalanche condition, resulting in an avalanche failure.

To prevent the avalanche failure associated with the gate oxide damage and enhance the avalanche capability of SiC trench MOSFET at the chip level, the uniformed electric field design should be introduced, corresponding to a uniformed temperature distribution. Furthermore, the low temperature condition of cryogenic applications is also helpful to improve the avalanche capability.

IV. Evaluation of Avalanche Capability

In order to further analyze and verify the avalanche failure mechanisms, in this section, the avalanche performance of SiC planar/trench MOSFETs are characterized at room temperature, and the avalanche failure mechanism is discussed. For fair comparison and analysis, the current/voltage levels of SiC planar and trench MOSFET are similar [31]-[32].

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A. Junction Temperature Extraction Method In UIS

The most avalanche failure or reliability issues are caused by overheating, particularly in the avalanche process with high instantaneous power. The calculation of internal temperature is critical for evaluating avalanche capability and analyzing the avalanche failure mechanism.

The transient thermal behavior of a power device can be simulated by using equivalent thermal-network, such as Foster-model (Fig. 7). The thermal impedance of a partial fraction model can be expressed as:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i (1 - e^{-\frac{t}{\tau_i}}) \quad (2)$$

whereas

$$\tau_i = R_i * C_i \quad (3)$$

where R_i and C_i are thermal resistance and thermal capacitance, corresponding to the thermal time τ_i. For an actual power device with the TO-247 packages, the fourth-order Foster-network is usually considered, associated with the physical structure of power chip, solder layer, the copper base frame, and CTE-matched EMC (epoxy molding compound).

Using the curve fitting tool within MATLAB, each component of *RC* thermal network can be extracted based on the transient thermal impedance ($Z_{th}(t)$) curve. The specific values of R and C for the SiC planar/trench MOSFET are listed in TABLE III. The larger minimum τ_i of SiC planar MOSFET implies a faster temperature increase, which has serious influence on short time scale. In comparison, the smaller total thermal resistance indicates a better heat dissipation capacity under long time scale.

B. Avalanche Performance of SiC Planar MOSFET

As shown in Fig. 8, the avalanche switching waveforms of SiC planar MOSFET are extracted while the peak avalanche current increases from 4.8 to 22.0 A. An avalanche failure is observed under I_{avp} condition of 22.0 A. The avalanche current drops first and rises again during the avalanche period, while the drain-source voltage of the SiC MOSFET drops to zero when the gate voltage changes.

By multiplying the transient avalanche voltage and current, the transient avalanche power loss under different current level are calculated, as illustrated in Fig. 9. At I_{avp} of 22.0 A, the maximum peak power loss (P_{avp}) is as large as 34.4 kW.

Combining the calculated transient avalanche power loss waveforms and the extracted thermal network, the transient temperature inside the SiC MOSFET can be extracted with circuit simulation software LTspice, as illustrated in Fig. 10. Firstly, establish the RC thermal network with the parameters listed in TABLE III. Secondly, use a current source to simulate the transient avalanche power loss waveforms illustrated in Fig. 9. Thirdly, use a DC voltage source to simulate the ambient temperature (298 K). Fourthly, obtain the transient junction temperature inside the SiC MOSFET with the transient simulation mode of LTspice.

When an avalanche failure occurs, the maximum junction temperature is elevated to 615.8 ℃, which is smaller than the melting point of aluminum (660 ℃) and the transition

TABLE III
THERMAL RESISTANCE AND CAPACITANCES OF TWO DUTS

Component (Unit)	SiC Planar MOSFET	SiC Trench MOSFET
C1 (s·W/K)	0.001034	0.001651
C2 (s·W/K)	0.003684	0.009627
C3 (s·W/K)	0.007963	0.08269
C4 (s·W/K)	0.182	0.177
R1 (K/W)	0.01178	0.06632
R2 (K/W)	0.03938	0.5151
R3 (K/W)	0.2778	0.1032
R4 (K/W)	0.3101	0.03017
R-square	**0.9999**	**0.9999**

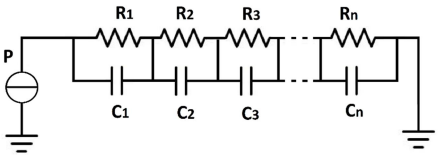

Fig. 7 Equivalent Foster-network of thermal system.

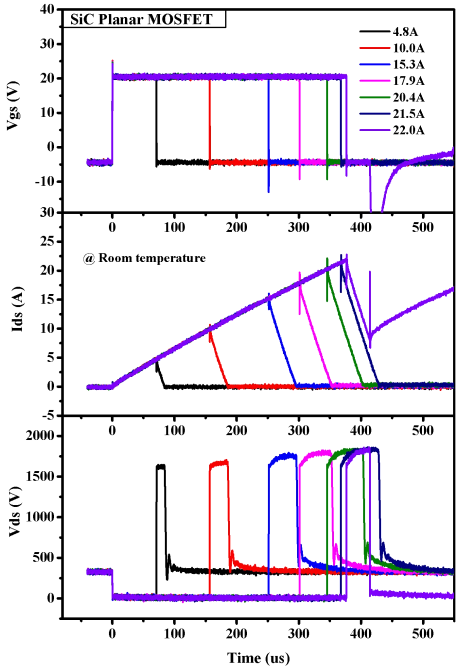

Fig. 8 Measured avalanche waveforms of SiC planar MOSFET with peak avalanche current increasing from 4.8 to 22A at room temperature. Measurement conditions: R_g = 3.3 Ω, V_{dc} = 320 V, C_{dc} = 42.3 uF and L = 5.886 mH.

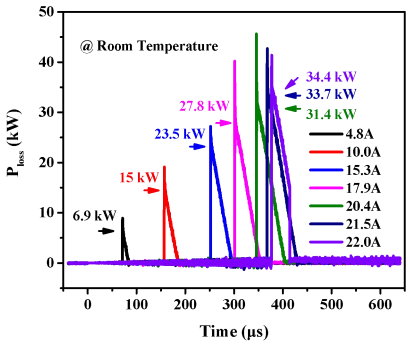

Fig. 9 Calculated transient power loss of SiC planar MOSFET with peak avalanche current increasing from 4.8 to 22A at room temperature.

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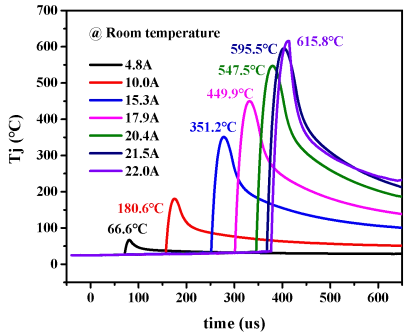

Fig. 10 Calculated transient junction temperature of SiC planar MOSFET with peak avalanche current increasing from 4.8 to 22 A at room temperature.

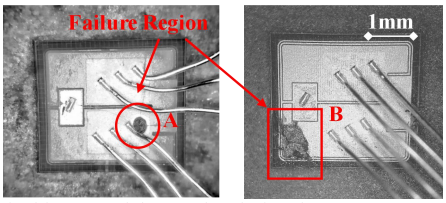

Fig. 11 Typical images of decapsulated SiC planar MOSFETs after single pulse UIS avalanche failure.

temperature of SiC material (1035 °C). Following the analysis in Section III. A. 3), the extremely high temperature causes the latch-up of parasitic BJT, resulting in an avalanche failure.

To further understand the avalanche failure mechanism, decapsulation of SiC planar MOSFET is performed after the avalanche failure. As illustrated in Fig. 11, although all solder joints of the bond wire are intact with the source/gate contact metallization, the active region of chip shows obvious burnt marks with two failure topographies. One topography (one round burned spot) is localized at the source terminal and in close proximity to one of the bond wires, as marked by "Failure Region A"; the other topography (irregular metalized burned areas) occurs at the left edge of the source metallization, as marked by "Failure Region B". In detail, the observations of failure sites show a serious burning center occurs in both topographies, which is thought to be caused by the high avalanche failure current flowing though the weak cells in power chip.

Combining with the TACD simulation results, experiment waveforms, transient temperature, and decapsulation images, the avalanche failure mechanism of SiC planar MOSFET can be verified as the latch-up of parasitic BJT, eventually resulting in a metallization of package material. To achieve an excellent avalanche capability in actual applications, the optimization of chip cell and reduction the operating temperature are two effective methods while considering on the chip level and circuits level.

C. Avalanche Performance of SiC Trench MOSFET

The UIS switching waveforms of SiC trench MOSFET are measured while the peak avalanche current increases from 2.9 to 9.9 A at the room temperature, as shown in Fig. 12. For the normal avalanche process (I_{avp} < 9.2 A), the avalanche current decreases to zero while the drain-source voltage shows a slight increase from 1762 to 1845V.

The avalanche failure waveforms are much different from that of SiC planar MOSFET when the SiC trench MOSFET is

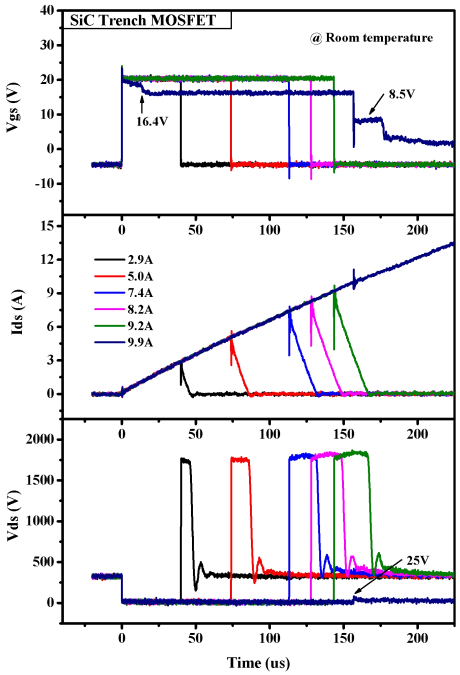

Fig. 12 Measured avalanche waveforms of SiC trench MOSFET with peak avalanche current increasing from 2.9 to 9.9A at room temperature. Measurement conditions: R_g = 3.3 Ω, V_{dc} = 320 V, C_{dc} = 42.3 uF and L = 5.886 mH.

characterized under the I_{avp} of 9.9 A. In initial phase (< 0 ns), the MOSFET has normal reverse electrical characteristics. The gate-source owns the voltage blocking capability of -5 V, while the V_{ds} is as high as 320 V to support DC bus voltage. In the first operation phase, i.e., between 0 and 156 us, albeit the MOSFET is turned on, the gate controllability of the SiC trench MOSFET shows some degradation. The V_{gs} drops to 16.4 V from 20 V, while the I_{ds} remains linearly increase and the V_{ds} is nearly about zero. Once the turn-off drive signal (-5 V) is applied at 156 us, the SiC trench MOSFET completely loses the gate control and the voltage block capability. The V_{ds} is not elevated to the theoretical avalanche voltage (> 1700 V), only about 25 V. The gate voltage decreases from 20 to 4.5V after 156 us, which is the only the voltage drops introduced by the gate current after the gate oxide layer is broken down.

In above UIS characterizations, the SiC trench MOSFET seems normal under I_{avp} of 9.2 A and the avalanche failure occurs at 9.9 A. To further determine whether the avalanche failure occurs at the end of the 9.2 A UIS test or the beginning of the 9.9 A UIS test, the gate oxide characteristics are measured after each single pulse UIS, as shown in Fig. 13. When the UIS is conducted under I_{avp} of 8.2 A, the blocking capability of gate oxide is almost identical to a fresh MOSFET. The gate leakage current is as small as 10 pA under the forward bias condition of 25 V. However, the higher I_{avp} introduces a more significant temperature accumulation effect, which enhances the electric field inside the MOSFET due to the higher temperature. After experiencing the UIS with I_{avp} of 9.2 A, the gate leakage current linearly increases up to 1 uA when the forward voltage is only 12.08 V. It indicates that the gate oxide layer has been partially broken down. Combining the TCAD simulation results, the break down point locates at the corner of the gate oxide. The gate oxide of SiC trench

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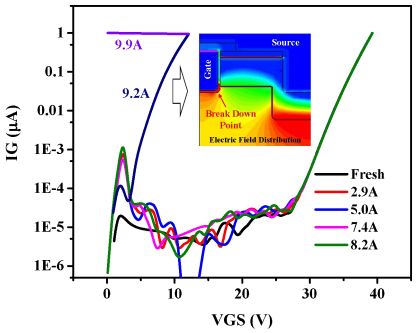

Fig. 13 Gate oxide characteristics of SiC trench MOSFET after experience each single pulse UIS with peak avalanche current increasing from 2.9 to 9.9A at room temperature.

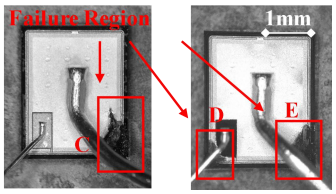

Fig. 14 Typical images of decapsulated SiC trench MOSFETs after single pulse UIS avalanche failure.

MOSFET is completely damaged after experiencing the 9.9 A UIS. The gate leakage current is close to the upper limit set by the test equipment even though the forward bias is very small. The high avalanche current after avalanche failure also causes a large-area metalized region on the surface of the power chip, as illustrated in Fig. 14.

Combining with the TACD simulation, the experiment waveforms, the analysis of gate oxide, and the decapsulation, it can be concluded that the extreme electric field at the corner of the gate oxide layer will severely limit the avalanche capability of SiC trench MOSFET. The optimization of chip cells is critical to improving the avalanche capability of SiC trench MOSFET, especially the advanced elimination design on the electric field.

D. Avalanche Capability Comparison

Due to the difference in device structures, the active areas of the SiC planar and trench MOSFETs are different, as 10.06 and 7.83 mm^2 respectively. To quantify the avalanche capability more fairly, the maximum peak avalanche current density (J_{mp}) is a reasonable parameter than the maximum peak avalanche current (I_{mp}). The J_{mp} of the SiC planar MOSFET is nearly about 2.165 A/mm^2, which is larger than that of SiC trench MOSFET, as 1.265 A/mm^2.

Although the two SiC MOSFETs have the same voltage and current rating, the avalanche capability of the SiC planar MOSFET is higher than that of the SiC trench MOSFET, as listed in TABLE IV. The main reason is that the gate oxide degradation of SiC trench MOSFET is caused by the high electric filed while the BJT latch-up of SiC planar MOSFET is closely related about the high avalanche current density.

V. Cryogenic Temperature Dependence of Avalanche Performance

In this section, the avalanche capability is evaluated and analyzed over the temperature range of 90 to 340 K. Particularly, since a large amount of heat is generated in each single pulse UIS, sufficient time is necessary before conducting the next measurement for the DUT to attain the equilibrium with the ambient temperature.

TABLE IV
AVALANCHE CAPABILITY COMPARISON

Device technology	SiC Planar MOSFET	SiC Trench MOSFET
Maximum Avalanche Current (A)	21.5~22.0	9.2~9.9
Die size (mm^2)	10.06	7.83
Maximum Avalanche Current Density (A/mm^2)	**2.14~2.19**	**1.17~1.26**

A. Temperature Dependence of Avalanche I-V

1) Temperature Dependence of SiC Planar MOSFET

The transient avalanche voltage significantly increases first then decreases under large I_{avp} conditions. Fig. 15(a) shows the avalanche voltage waveforms of SiC planar MOSFET at 90 K. In the power inductor charging phase, the small increase of junction temperature corresponds to an almost constant avalanche voltage, as illustrated with "line a". In comparison, the peak avalanche voltage (V_{avp}) rapidly rises with I_{avp} as illustrated with "line b". The avalanche voltage reaches 1790.2 V when an avalanche failure occurs, which implies the highest junction temperature.

As for the avalanche failure introduced by BJT latch-up, theoretically, the critical temperature point associated with the avalanche failure would decrease under cryogenic temperature while companying with a larger peak of avalanche current. Under low temperature, a larger temperature margin indicates that SiC MOSFET can withstand a higher peak value of avalanche current, corresponding to a higher avalanche current density. The larger horizontal component of the avalanche current introduces an increased voltage drop when it flows through the body resistance, as shown in the light blue area in Fig. 16. Considering the positive temperature coefficient of R_b and V_{bi} of $P_{body}N_{source}$ junction, avalanche failure will be triggered at a lower temperature point, companying with a larger peak of avalanche current.

The single pulse UIS characterizations are carried out to establish the avalanche operating boundary (AOB) of SiC planar MOSFET. The V_{avp} under each I_{avp} condition is extracted when the temperature changes over the temperature range of 90 to 340 K, as illustrated in Fig. 15(b). The V_{avp} almost linearly increases with I_{avp}. Meanwhile, I_{mp} with negative temperature coefficient decreases to 21.0 A at 340 K from 24.2 A at 90 K while the V_{mp} with positive temperature coefficient increases from 1790.2 to 1822.0 V over the temperature range of 90 to 340 K. The AOB of SiC planar MOSFET is shown with the dashed line in Fig. 15(b) over the cryogenic temperature range.

Above temperature dependence of AOB is fully consistent with the temperature characteristics of the BJT latch-up effect. Clearly, the avalanche capability of SiC planar MOSFET is enhanced under cryogenic temperature.

2) Temperature Dependence of SiC Trench MOSFET

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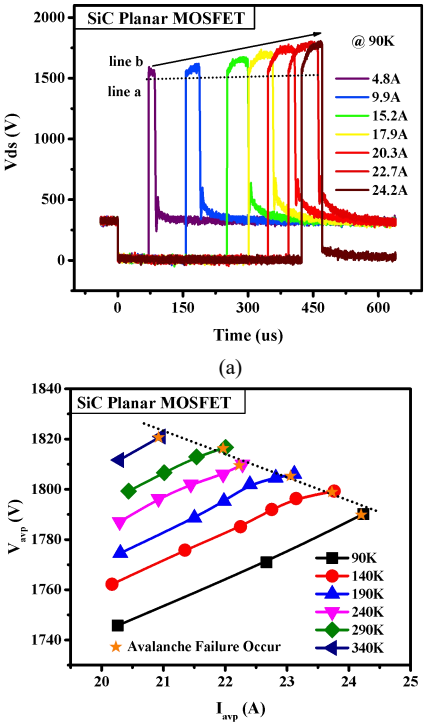

Fig. 15 The (a) measured avalanche voltage waveforms of SiC planar MOSFET with peak avalanche current increasing from 4.8 to 24.2 A at 90 K, and the (b) extracted peak avalanche voltage (V_{avp}) under different temperature and peak avalanche current (I_{avp}). Measurement conditions: R_g = 3.3 Ω, V_{dc} = 320 V, C_{dc} = 42.3 uF and L = 5.88 6 mH.

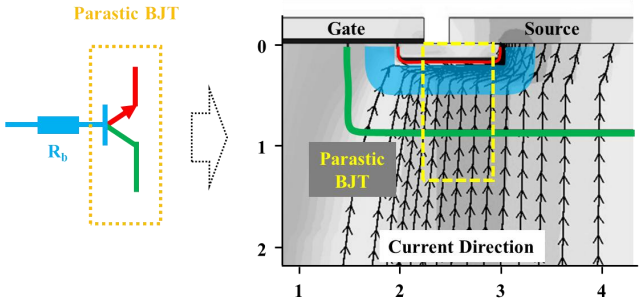

Fig. 16 The physical correspondence between the parasitic BJT with body resistance (R_b) and the internal region of the SiC planar MOSFET.

For the signal pulse UIS under 90K condition, the initial avalanche voltage of SiC trench MOSFET almost remains constant while the V_{avp} linearly rises, as illustrated with "line a" and "line b" in Fig. 17(a). When an avalanche failure occurs at I_{avp} of 14.4 A, the transient avalanche voltage reaches the maximum value, 1858.8 V.

Regarding the avalanche failure associated with the degradation of gate oxide, the corresponding internal electric field distribution should be consistent under different ambient temperatures when SiC Trench MOSFET fails, as illustrated in Fig. 13. Under cryogenic temperature, an elevated temperature margin implies a large peak value of avalanche current that the MOSFET can withstand without avalanche failure. Thereby, the avalanche current density is elevated and the hot carriers level is enhanced at the corners of the gate oxide layer. Due to the more deteriorating electrical environment of the oxide

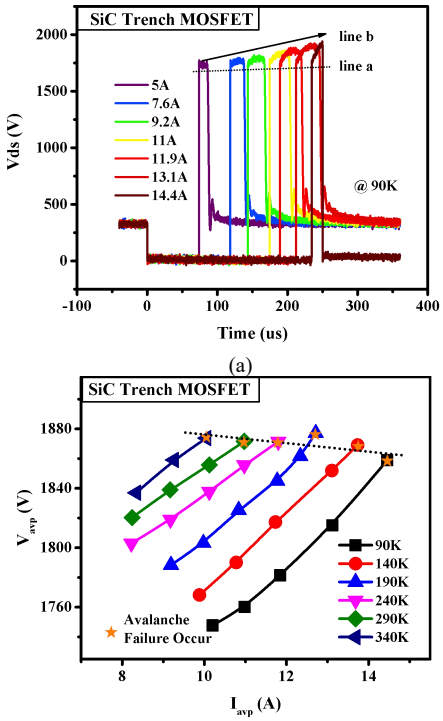

Fig. 17 The (a) measured avalanche voltage waveforms of SiC trench MOSFET with peak avalanche current increasing from 5.0 to 14.4A at 90 K, and the the (b) extracted peak avalanche voltage (V_{avp}) under different temperature and peak avalanche current (I_{avp}). Measurement conditions: R_g = 3.3 Ω, V_{dc} = 320 V, C_{dc} = 42.3 uF and L = 5.886 mH.

layer, the critical field strength that the device can withstand is slightly decreased as the temperature decreases, companying with a larger peak of avalanche current.

As illustrated in Fig. 17(b), the V_{avp} is almost constant for all temperature cases. The variation of V_{avp} is just 18.3 V when the I_{mp} decreases to 10.1 A at 340 K from 14.2 A at 90 K. The almost constant V_{avp} indicates that the internal electric field distribution of under different operation temperatures is almost the same when an avalanche occurs. The above temperature dependence is fully consistent with the analysis in Section III. B. 3). This result also further validates the correctness of the avalanche failure mechanism related to gate oxide breakdown.

The AOB of the SiC trench MOSFET is as shown with the dashed line in Fig. 17(b) over the cryogenic temperature range. The larger I_{mp} implies that the avalanche capability of SiC trench MOSFET is enhanced at cryogenic temperature.

3) Discussion of the avalanche operating boundary (AOB)

Over the temperature range of 90 to 340 K, the avalanche operating boundary of SiC planar/trench MOSFET is extracted based on single pulse UIS characterizations, which has great application value.

Firstly, the cryogenic AOB curve quantitatively illustrates the temperature dependence of avalanche voltage and avalanche current at the same time, which results could help the engineer to comprehensively evaluate the avalanche performance of SiC MOSFET under the cryogenic conditions.

Secondly, the cryogenic AOB curve can clearly reflect the main limitation of avalanche capability. The larger coefficient between the V_{mp} and the I_{mp} indicates that the avalanche

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capability limitation is closely associated with the avalanche current distribution inside SiC MOSFET. To improve the avalanche capability, attention should be paid to the optimization on the avalanche current path. In comparison, a smaller coefficient corresponds to the avalanche failure mechanism related to the internal electric field distribution inside SiC MOSFET. The device structure optimization should be focused on the uniformed electric field design. Comparing with SiC planar MOSFET, the small coefficient of SiC trench MOSFET indicates that the extremely high electric field would contribute to the avalanche failure.

Noted that the above analysis method is suitable for all power switches, beyond above two SiC MOSFET.

B. Temperature Dependence of Avalanche Capacity

1) Temperature effect on avalanche currrent

In order to fairly evaluate the avalanche capabilities of two MOSFETs, the maximum peak avalanche current density is used, referring to the current density that the DUT can withstand without avalanche failure. The J_{mp} can eliminate the non-ideal factors associated with the difference in chip size.

The temperature influence on avalanche voltage and current is summarized and listed in TABLE V. For SiC planar MOSFET, the V_{mp} increment is 31.8 V over the temperature range of 90 to 340 K. In comparison, the increment of SiC trench MOSFET is only 18.4 V. The opposite situation occurs for avalanche current characteristics. The variation of J_{mp} reduction of SiC planar MOSFET (0.32 A/mm^2) is much smaller than that of SiC trench MOSFET (0.52 A/mm^2).

2) Temperature effect on avalanche energy

Based on the single pulse UIS, the temperature dependence of maximum avalanche energy (E_{avm}) is extracted over the temperature range of 90 to 340 K. In addition, a Si CoolMOS is selected and characterized to highlight the application potential of SiC MOSFET. The Si CoolMOS has the same current rate with two SiC MOSFETs [33].

As shown in Fig. 18. the E_{avm} of three DUTs decreases linearly when the temperature increases from 90 to 340 K. In order to accurately describe the temperature characteristics of avalanche capability, a linear model is proposed as follows:

$$E_{avm}(T) = K(T - RT) + E_{avm-RT} \quad (4)$$

where K is the temperature coefficient of E_{avm}, RT represents the room temperature, i.e. 300 K, $E_{avm\text{-}RT}$ is the maximum avalanche energy under room temperature condition. For SiC planar MOSFET and SiC trench MOSFET, the temperature coefficients are -1.71 and -1.23 mJ/K, respectively. Meanwhile, the E_{avm} of SiC planar MOSFET (1.42 J at 290 K) is nearly four times larger than that of SiC trench MOSFET (0.35 J at 290 K). For Si CoolMOS, the temperature coefficient of E_{avm} is as large as -11.38 mJ/K while the E_{avm} decreases from 3.47 to 0.65 J.

TABLE V
AVALANCHE CHARACTERISTIC
UNDER TEMPERATURE RANGE OF 90 TO 340 K

Device technology	V_{mp} Increment (V)	J_{mp} Reduction (A/mm^2)
SiC Planar MOSFET	31.8 (from 1790.2 to 1822.0)	0.32 (from 2.41 to 2.09)
SiC Trench MOSFET	**18.4** (from 1858.8 to 1877.2)	0.52 (from 1.81 to 1.29)

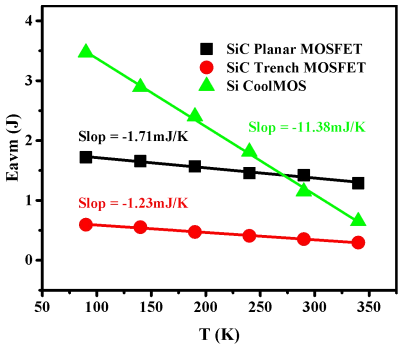

Fig. 18 The extracted maximum avalanche energy (E_{avm}) over temperature range of 90 to 340K. Measurement conditions: R_g = 3.3 Ω, V_{dc} = 320 V, C_{dc} = 42.3 uF and L = 5.886 mH.

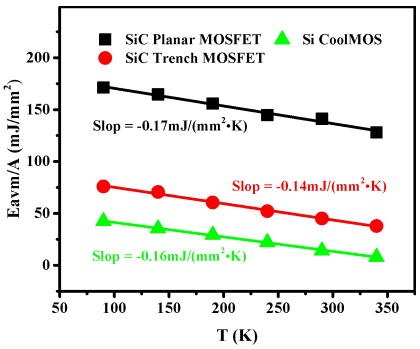

Fig. 19 The extracted maximum avalanche energy density (E_{max}/A) over temperature range of 90 to 340K. Measurement conditions: R_g = 3.3 Ω, V_{dc} = 320 V, C_{dc} = 42.3 uF and L = 5.886 mH.

To essentially reflect the temperature dependence of the avalanche capability, the chip area is taken into consideration. Similar to the temperature dependence of E_{avm}, the maximum avalanche energy density (E_{avm}/A) also has a good linear relationship with temperature, as shown in Fig. 19. Above relationship can be expressed by a linear function, as follows:

$$E_{avm} / A(T) = K'(T - RT) + E / A_{avm-RT} \quad (5)$$

where K' is the temperature coefficient of E_{avm}/A, $E/A_{avm\text{-}RT}$ is the maximum avalanche energy density at room temperature. The characterization results illustrate that K' of three MOSFETs are almost the same, which are -0.17, -0.16, and -0.14 mJ/(mm^2•K), respectively. In comparison, the absolute values of E_{avm}/A are quite different. At 90 K, the E_{avm}/A of SiC planar MOSFET, SiC trench MOSFET, and Si CoolMOS are 171.24, 75.94, and 42.48 mJ/mm^2, respectively.

The cryogenic condition enhances the avalanche capability of SiC MOSFETs. Due to the difference in avalanche failure mechanism, the E_{avm}/A of SiC planar MOSFET is much larger than that of SiC trench MOSFET. Overall, the larger E_{avm}/A of SiC MOSFET indicates that the avalanche capability of SiC MOSFET is better than Si CoolMOS.

VI. CONCLUSION

Based on a customized self-built single pulse UIS characterization platform, for the first time, the temperature dependence of the avalanche capability of SiC planar/trench MOSFETs is systematically characterized and analyzed over

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temperature range of 90 to 340 K. The quantitative results reveal that the avalanche capability of SiC MOSFETs is greatly enhanced under cryogenic conditions. At 90 K, the J_{mp} of SiC planar and trench MOSFETs is as large as 2.41 and 1.81 A/mm^2, while the E_{max}/A increases up to 171.24 and 75.94 mJ/mm^2. The excellent avalanche performance of SiC MOSFETs indicates the great potential in superconductivity related applications and aerospace applications.

Combining with various analysis methods, the essential mechanism and temperature dependence of avalanche failure of SiC MOSFETs are further explored over the cryogenic temperature range. The latch-up of parasitic BJT is the major limitation of the SiC planar MOSFET, while the gate oxide degradation dominates avalanche failures of the SiC trench MOSFET. Regarding the difference of avalanche failure mechanisms, the avalanche capability of SiC planar MOSFET is much better than that of SiC trench MOSFET. To improve the avalanche capability, the advanced elimination concept on the electric field approach should be taken for the design of SiC planar MOSFET, while the optimization design with the purpose of uniform temperature distribution approach should be taken for SiC trench MOSFET.

In addition, a safe avalanche operating boundary (AOB) of SiC MOSFETs is established over the cryogenic temperature range. The large absolute temperature coefficients, 0.17 and 0.14 mJ/(mm^2•K), indicates that the temperature reduction will greatly improve the avalanche capability of SiC MOSFETs. Importantly, the analysis method and avalanche performance model can accurately evaluate and quantitatively predict the avalanche capability of SiC planar/trench MOSFETs under cryogenic conditions, which has great application value for the design of cryogenic converters.

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